

FIG. 1

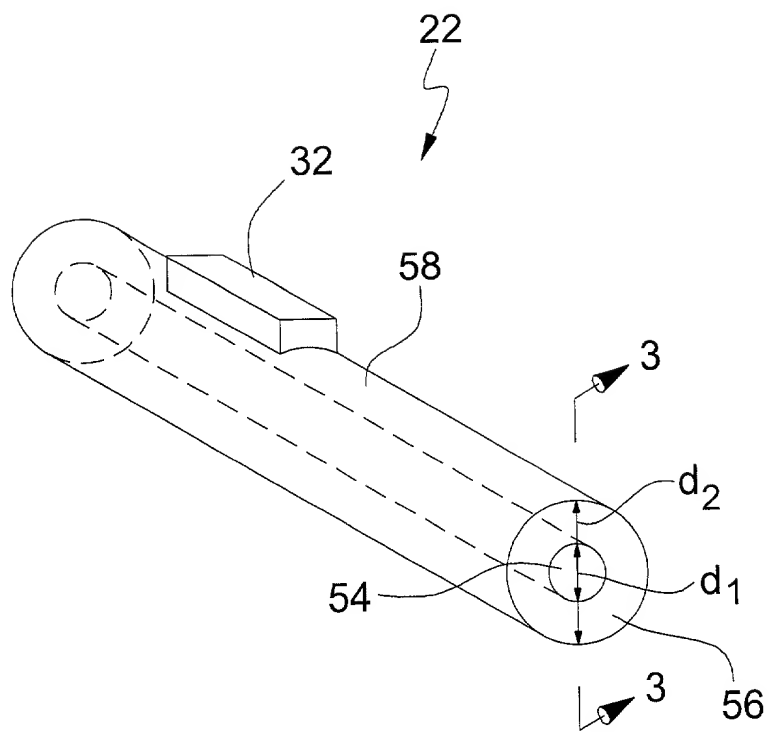


FIG. 2

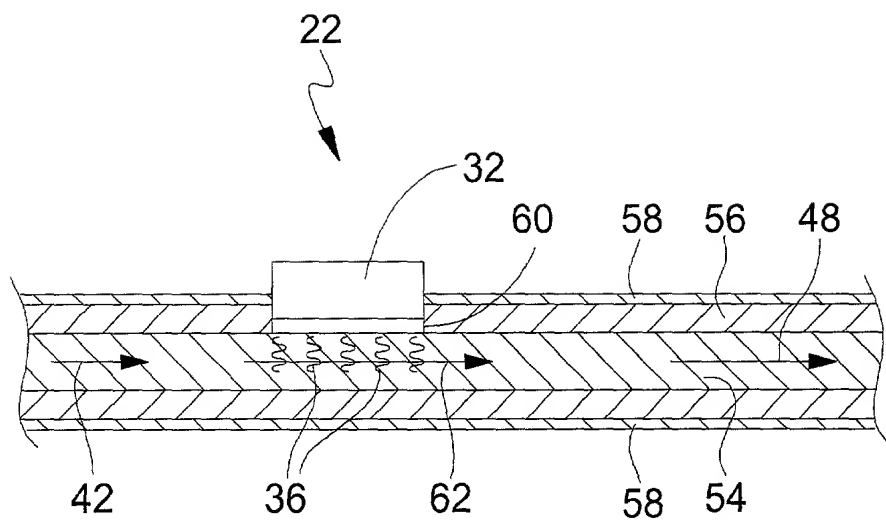
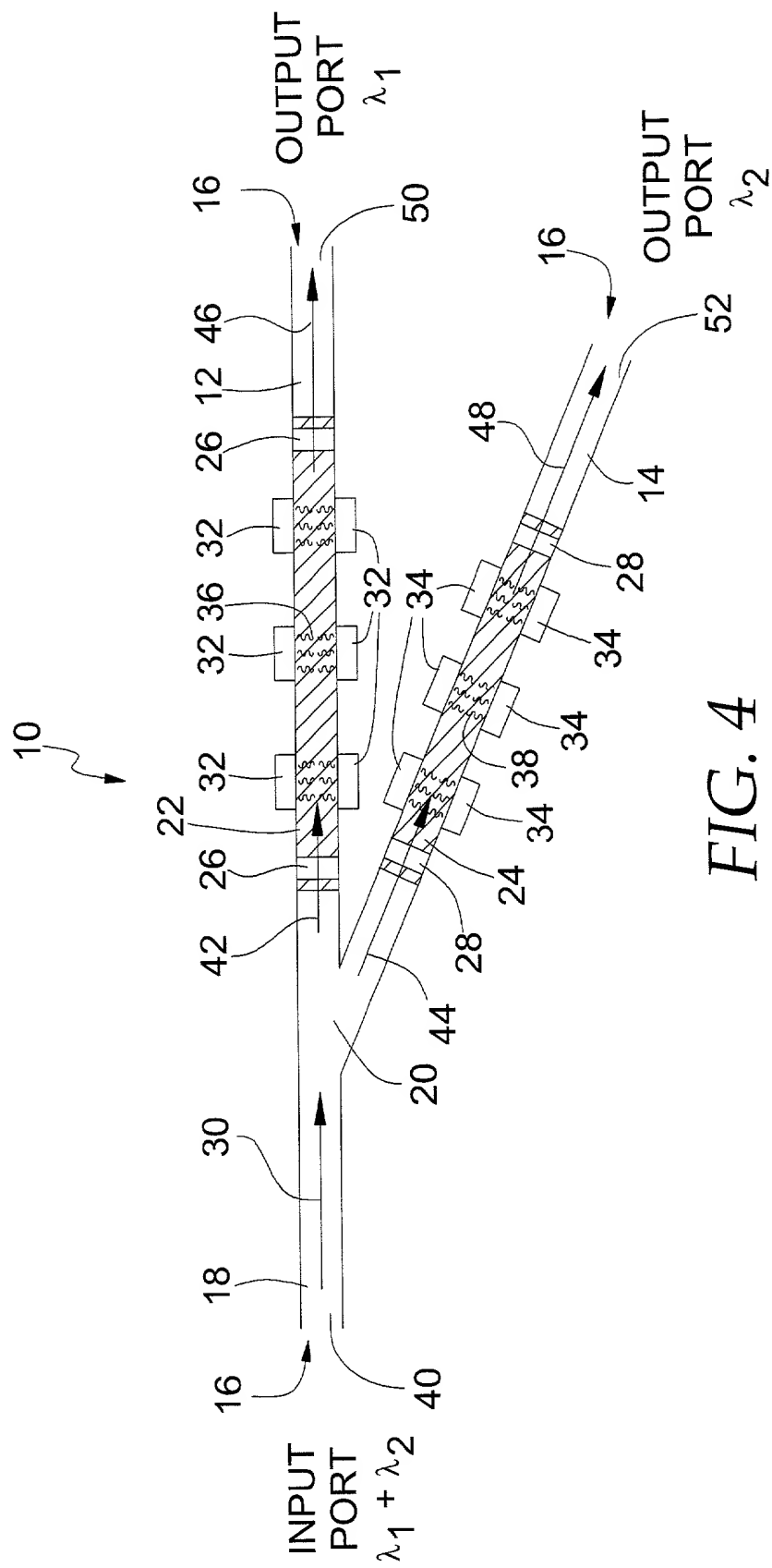
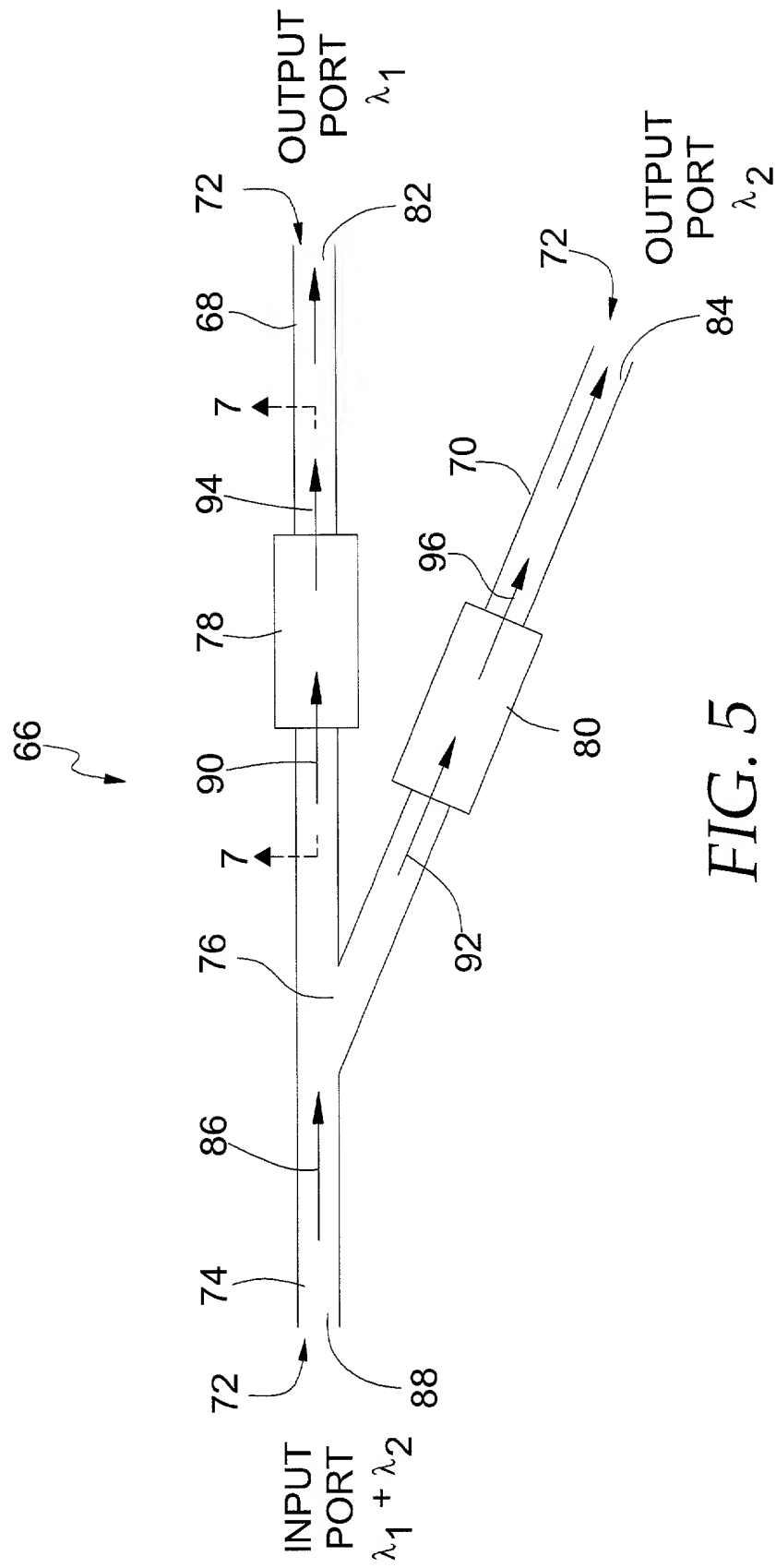


FIG. 3





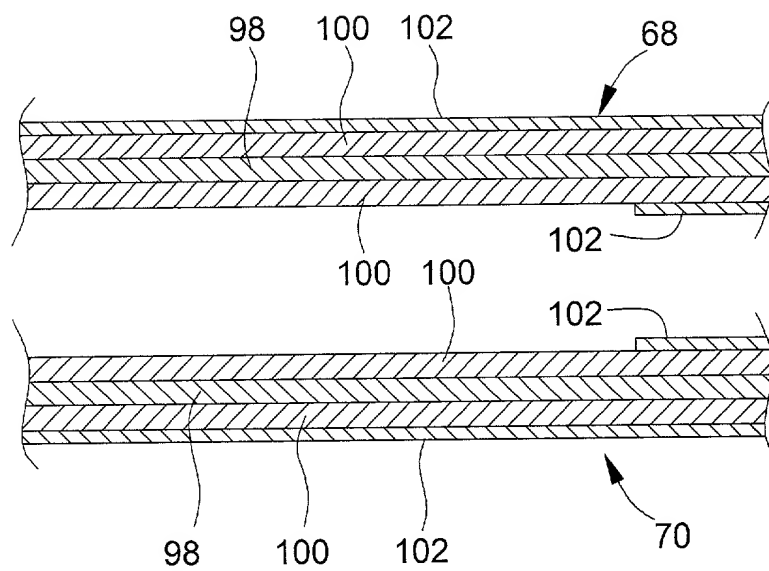


FIG. 6A

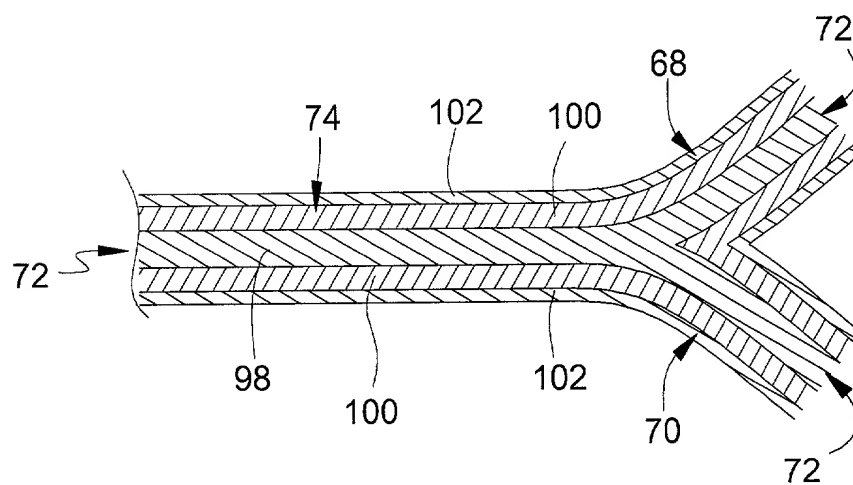


FIG. 6B

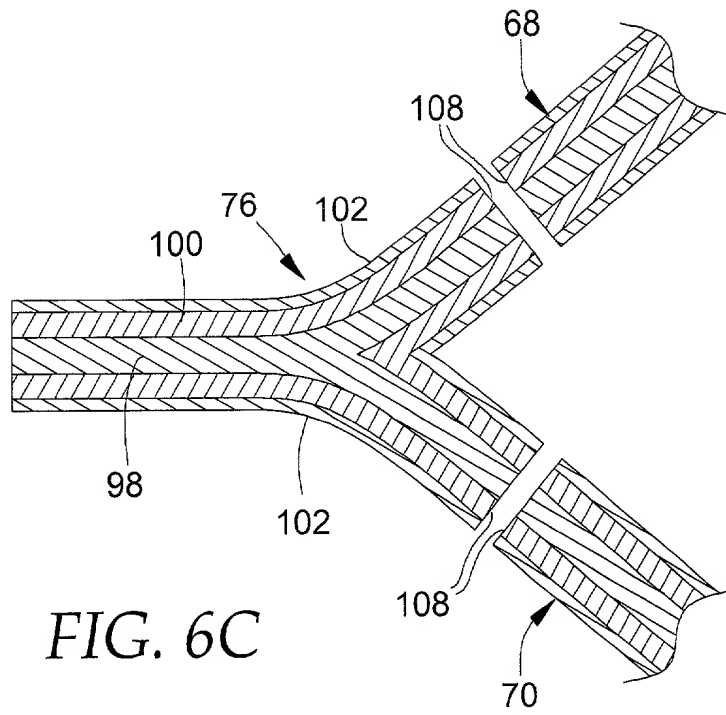


FIG. 6C

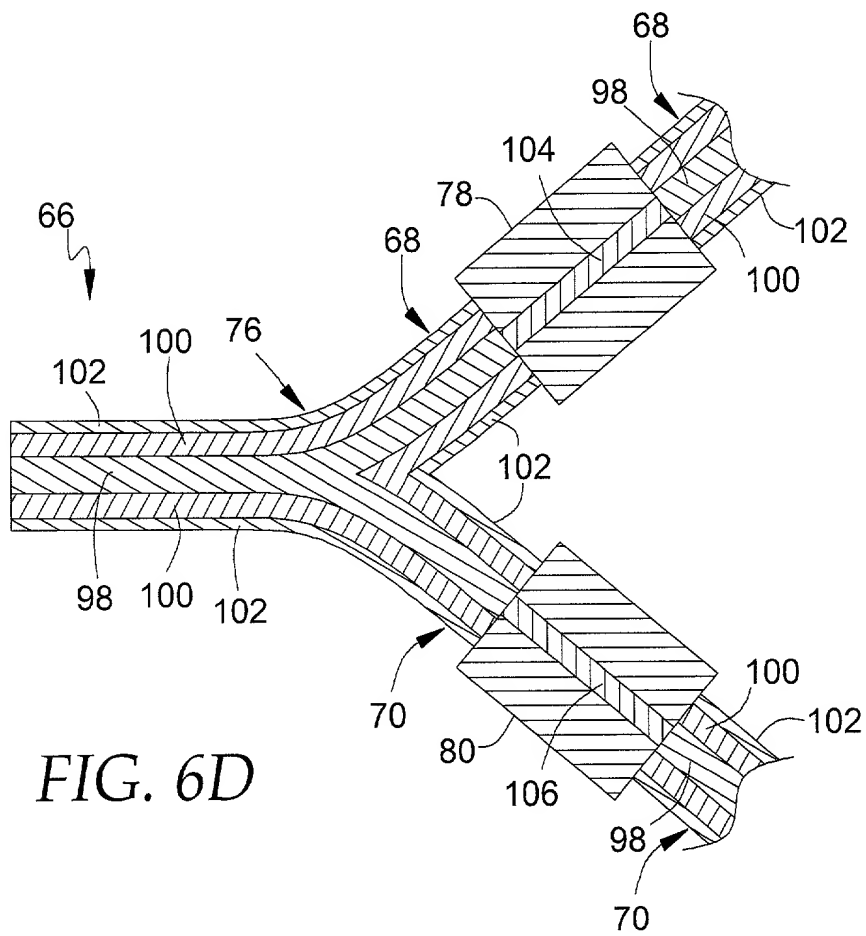


FIG. 6D

FIG. 7 is a cross-sectional view of a device 100 in accordance with an embodiment of the present disclosure. The device 100 includes a substrate 90, a first layer 98, a second layer 102, a third layer 60, a fourth layer 100, a fifth layer 94, a sixth layer 98, a seventh layer 102, and an eighth layer 68. The device 100 also includes a central region 110, a first side region 114, and a second side region 114. The device 100 is configured to receive an electrical current 116. The device 100 is configured to have a first thickness d_1 and a second thickness d_2 .

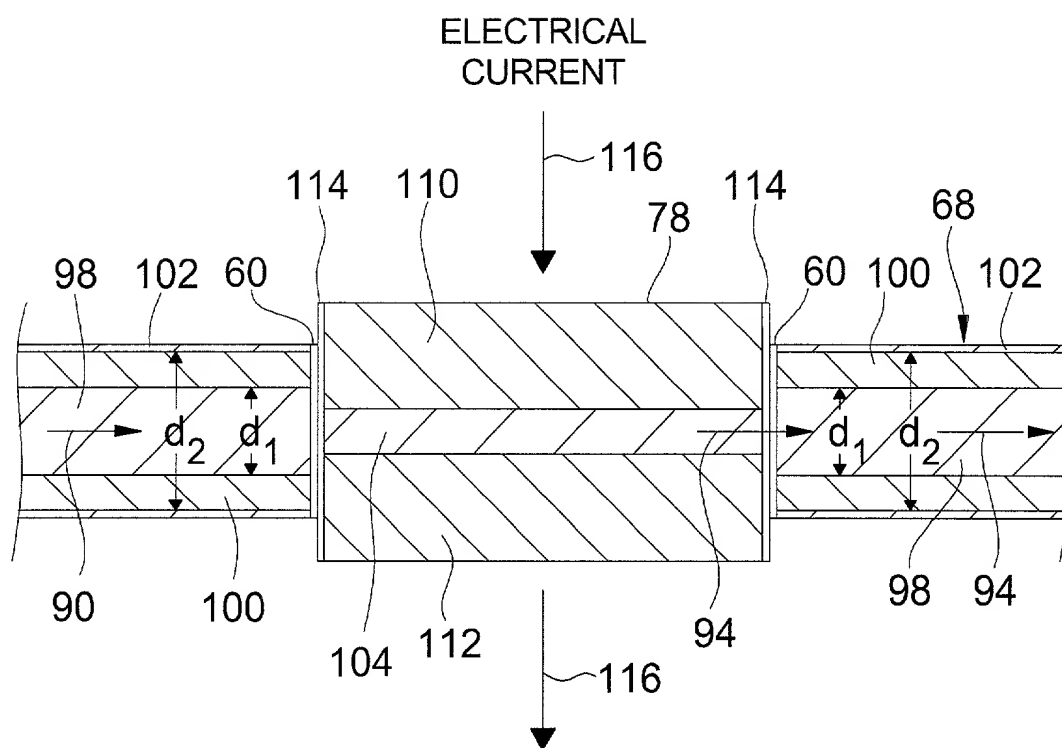
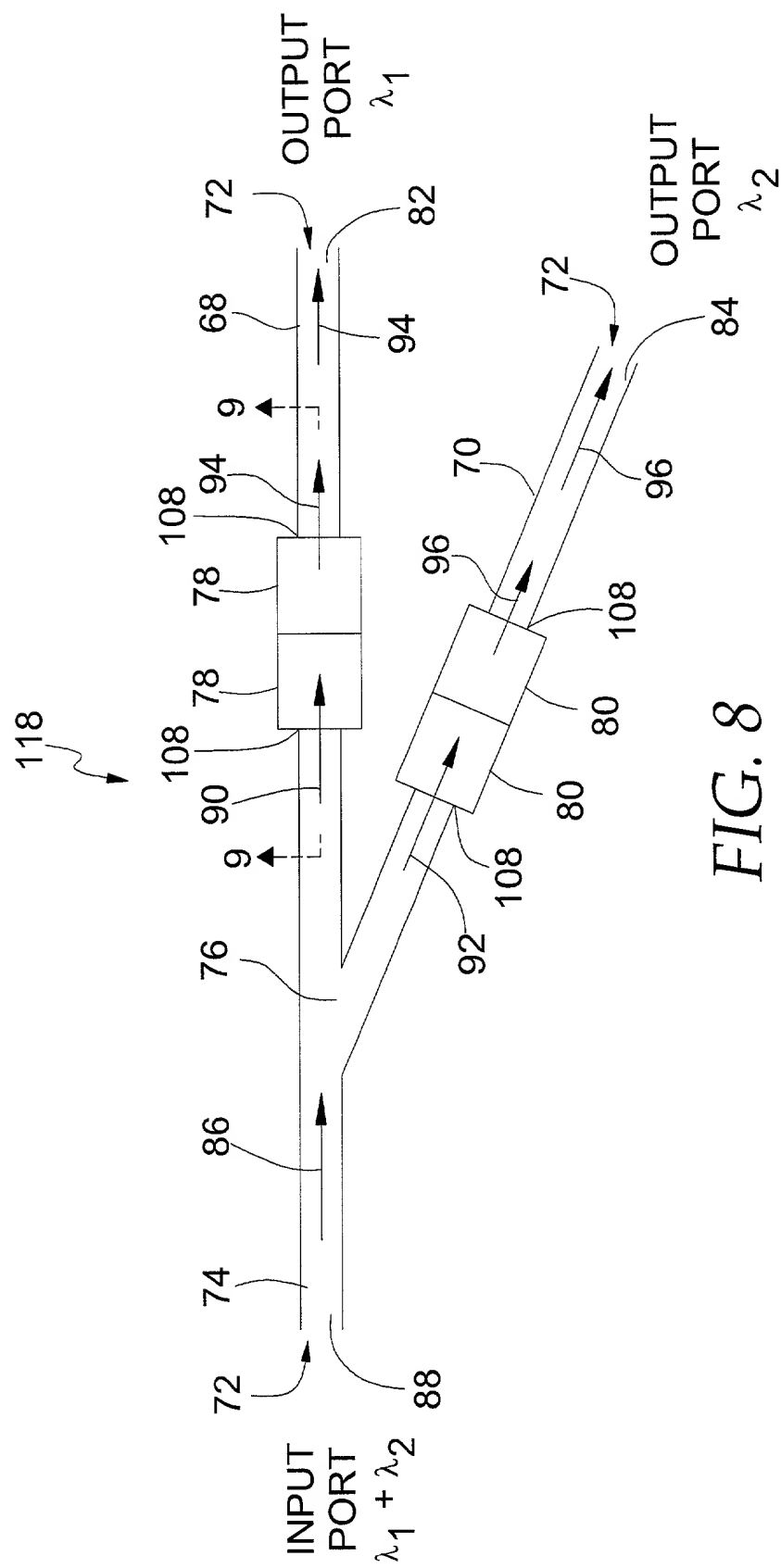


FIG. 7



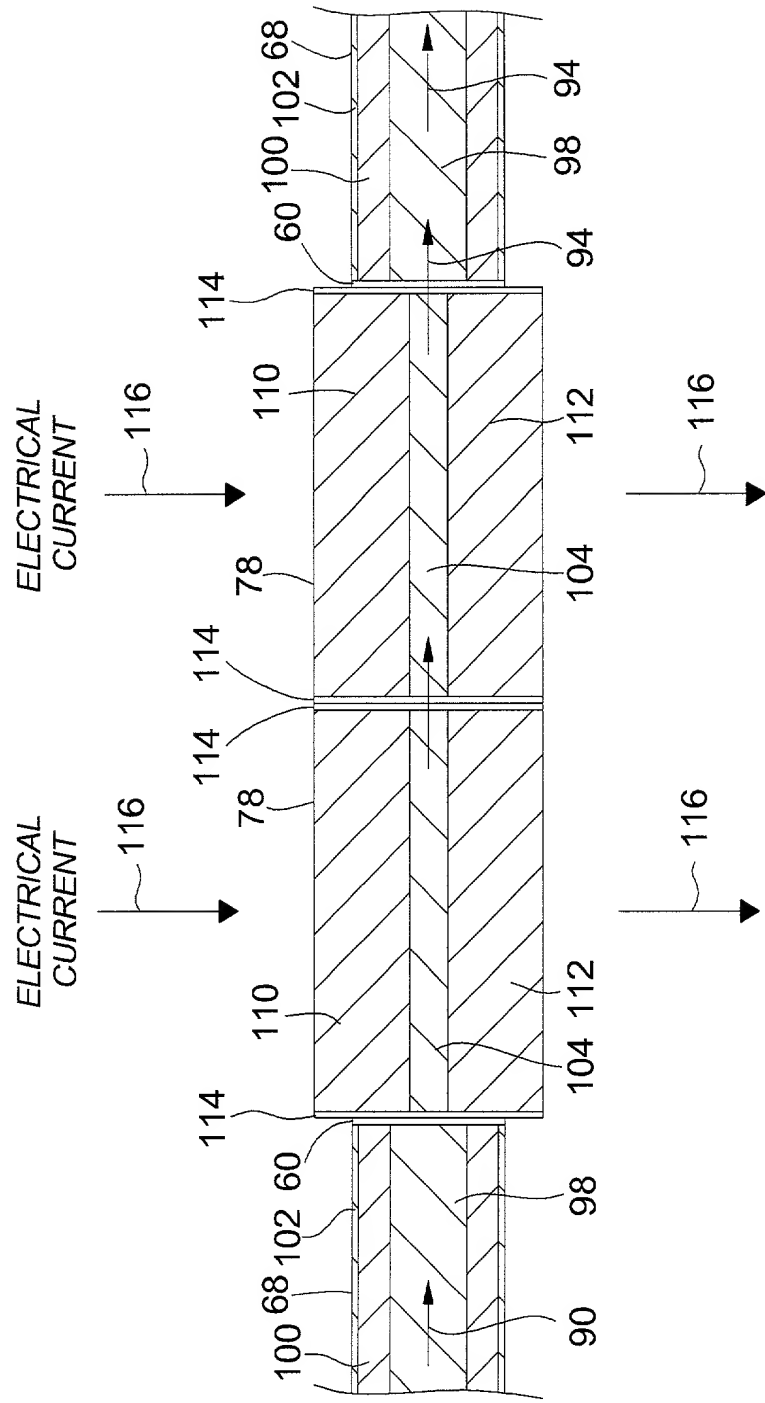


FIG. 9

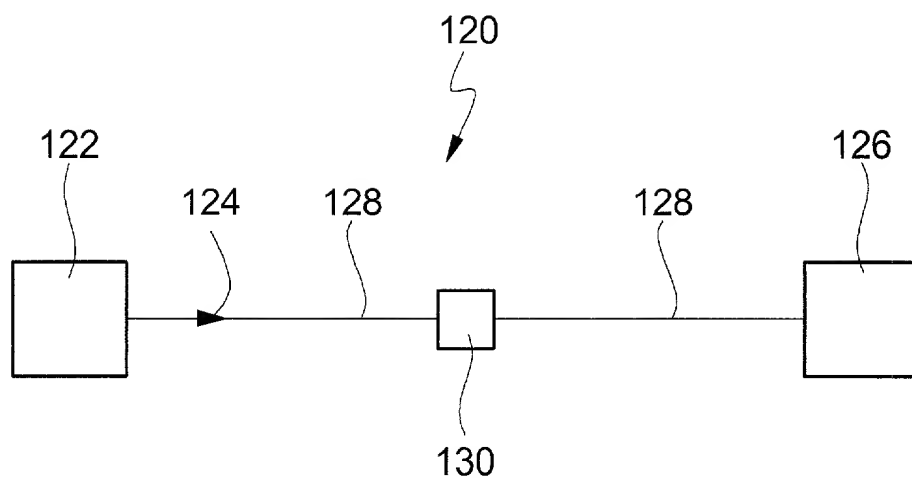


FIG. 10